CLAIMS

What is claimed is:

1. A system which indicates semiconductor device fabrication defects comprising:

test data corresponding to testing of a plurality of fuses, each one of the plurality of fuses residing on a different one of a plurality of semiconductor devices and each one of the plurality of fuses having a common location on the semiconductor devices; and

a memory with logic configured to determine from the test data which of the plurality of fuses are defective fuses, and further configured to specify on an output report the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion of the plurality of fuses.

2. The system of claim 1, further comprising a fuse test device configured to test the plurality of fuses.

3. The system of claim 2, wherein the fuse test device further comprises a fuse test unit configured to test the plurality of fuses when the semiconductor device resides on a wafer.

4. The system of claim 2, wherein the fuse test device further comprises a fuse test unit configured to test the plurality of fuses when the semiconductor device resides on a die.

5. The system of claim 2, wherein the fuse test device further comprises a fuse test unit configured to test the plurality of fuses when the semiconductor device resides on an integrated circuit chip.

6. The system of claim 2, wherein the fuse test device further comprises a fuse test unit configured to test the plurality of fuses when the semiconductor device resides on a circuit board.

7. A method for indicating semiconductor device fabrication defects, the method comprising:

retrieving test data corresponding to test results from a plurality of fuses, each one of the plurality of fuses residing on a different one of a plurality of semiconductor devices and each one of the plurality of fuses having a common location on the semiconductor devices;

determining from the test data which of the plurality of fuses are defective fuses; and

specifying on an output report the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion of the plurality of fuses.

8. The method of claim 7, further comprising specifying the predefined portion as a percentage.

9. The method of claim 7, further comprising:

retrieving the test data corresponding to the test results from a plurality of second fuses, each one of the plurality of second fuses residing on a different one of the semiconductor devices and each one of the plurality of second fuses having a second common location on the semiconductor devices;

determining from the test data which of the plurality of second fuses are defective second fuses; and

specifying on the output report the second common location of the determined defective second fuses when a number of the defective second fuses are at least equal to the predefined portion of the plurality of second fuses.

10. The method of claim 7, further comprising:

retrieving the test data corresponding to the test results from a plurality of fuse arrays, each one of the fuse arrays having a plurality of array fuses and each one of the plurality of fuse arrays having a common fuse array location on the semiconductor devices;

determining from the test data which of the plurality of array fuses are defective array fuses; and

specifying on the output report the common fuse array location when a number of the defective array fuses are at least equal to a predefined portion of the array fuses.

11. The method of claim 7, further comprising:

retrieving the test data corresponding to the test results from a plurality of fuse registers, each one of the fuse registers having a plurality of register fuses and each one of the plurality of fuse registers having a common fuse register location on the semiconductor devices;

determining from the test data which of the plurality of register fuses are defective register fuses; and

specifying on the output report the common fuse registers location when a number of the defective register fuses are at least equal to a predefined portion of the register fuses.

12. The method of claim 7, further comprising:

retrieving the test data corresponding to the test results from a grouping of fuses, each one of the grouped fuses in the grouping of fuses having a common location on the semiconductor devices;

determining from the test data which of the grouped fuses are defective; and

specifying on the output report the common location when a number of the defective grouped fuses are at least equal to a predefined portion of the grouped fuses.

13. The method of claim 7, further comprising displaying the output report.

14. The method of claim 7, further comprising printing the output report.

15. The method of claim 7, further comprising testing the plurality of fuses.

16. A system for identifying semiconductor device fabrication defects, comprising:

means for retrieving test data corresponding to test results from a plurality of fuses, each one of the plurality of fuses residing on a different one of a plurality of semiconductor devices and each one of the plurality of fuses having a common location on the semiconductor devices;

means for determining from the test data which of the plurality of fuses are defective fuses;

means for generating an output report the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion of the plurality of fuses; and

means for displaying the output report.

17. The system of claim 16, further comprising:

means for retrieving the test data corresponding to the test results from a plurality of second fuses, each one of the plurality of second fuses residing on a different one of the semiconductor devices and each one of the plurality of second fuses having a second common location on the semiconductor devices;

means for determining from the test data which of the plurality of second fuses are defective second fuses; and

means for specifying on the output report the second common location of the determined defective second fuses when a number of the defective second fuses are at least equal to the predefined portion of the plurality of second fuses.

18. The system of claim 16, further comprising:

means for retrieving the test data corresponding to the test results from a plurality of fuse arrays, each one of the fuse arrays having a plurality of array fuses and each one of the plurality of fuse arrays having a common fuse array location on the semiconductor devices;

means for determining from the test data which of the plurality of array fuses are defective array fuses; and

means for specifying on the output report the common fuse array location when a number of the defective array fuses are at least equal to a predefined portion of the array fuses.

19. The system of claim 16, further comprising:

means for retrieving the test data corresponding to the test results from a plurality of fuse registers, each one of the fuse registers having a plurality of register fuses and each one of the plurality of fuse registers having a common fuse register location on the semiconductor devices;

means for determining from the test data which of the plurality of register fuses are defective register fuses; and

means for specifying on the output report the common fuse register location when a number of the defective register fuses are at least equal to a predefined portion of the register fuses.

20. The system of claim 16, further comprising:

means for retrieving the test data corresponding to the test results from a grouping of fuses, each one of the grouped fuses in the grouping of fuses having a common location on the semiconductor devices;

means for determining from the test data which of the plurality of grouped fuses are defective; and

means for specifying on the output report the common location when a number of the defective grouped fuses are at least equal to a predefined portion of the grouped fuses.

21. A computer-readable medium having a program for indicating semiconductor device fabrication defects, the program comprising logic configured to perform:

receiving from a memory test data corresponding to test results from a plurality of fuses, each one of the plurality of fuses residing on a different one of a plurality of semiconductor devices and each one of the plurality of fuses having a common location on the semiconductor devices;

determining from the test data which of the plurality of fuses are defective fuses; and

specifying on an output report the common location of the determined defective fuses when a number of the defective fuses are at least equal to a predefined portion of the plurality of fuses.